Q.P. Code: 19EC0401 **R19**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech I Year II Semester Regular Examinations October-2020

SWITCHING THEORY & LOGIC DESIGN

(Electronics & Communication Engineering)

Time: 3 hours Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1 **a** Simplify the following Boolean expressions to minimum no. of literals. **6M**

i) ABC+A'B+ABC'

ii) (BC'+A'D)(AB'+CD')

iii) x'yz+xz

iv) xy+x(wz+wz'

b Obtain the Dual of the following Boolean expressions. **6M**

i) AB+A(B+C)+B'(B+D)

ii) A+B+A'B'C

iii) A'B+A'BC'+A'BCD+A'BC'D'E

iv) ABEF+ABE'F'+A'B'EF

OR

2 **a** Convert the following to Decimal and then to Octal. **6M**

i) $(42341)_6$

ii) $(10010011)_2$.

b Convert the following to Decimal and then to Hexadecimal. **6M**

i) $(1234)_8$

ii) $(11001111)_2$

UNIT-II

3 Simplify the following expression using tabulation technique. **12M**

$F=\Sigma m(0,1,2,8,9,15,17,21,24,25,27,31)$

OR

4 **a** Simplify the following expression using the K-map for the 3-variable. **6M**

Y = AB'C+A'BC+A'B'C+A'B'C'+AB'C'

b Simplify the Boolean function $F(A,B,C,D)=\Sigma(1,3,7,11,15)+d(0,2,5)$ **6M**

UNIT-III

5	**a**	Design & implement Full Adder with truth table.	**6M**
	b	Design & implement Full Subtractor with truth table.	**6M**

OR

6	**a**	Design & implement a 4-bit Binary-To-Gray code converter.	**6M**
	b	Design a 4 bit binary-to-BCD code converter	**6M**

UNIT-IV

7	**a**	Draw the logic symbol, characteristics table and derive characteristics equation of JK flip flop.	**6M**
	b	Design T Flip Flop by using JK Flip Flop and draw the timing diagram.	**6M**

OR

8		A sequential circuit with two D-flip flops A and B, two inputs 'x' and 'y' and one output 'z' is specified by the following next state and output equation. A(t+1) = x'y+xA, B(t+1) = x'B+xA and Z = B **i)** Draw the logic diagram of the circuit. **ii)** List the state table and draw the corresponding state diagram.	**12M**

UNIT-V

9		Discuss Mealy & Moore Machine models of sequential machines.	**12M**

OR

10		Implement the following Boolean function usingPLA i) F1= Σm(0,1,2,3,8,10,12,14) ii) F2 = Σm(0,1,2,3,4,6,8,10,12,14).	**12M**

*** END ***